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Development of Si-W Transient Tolerant Plasma Facing Material

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Abstract. Solid W is projected as the preferred plasma facing material. Unfortunately, W surfaces could suffer radiation damage under DT operation and will melt under Type-I edge localized modes and disruption events. A possible approach is the use of a low-Z sacrificial material, like Si deposited on the W-surface to withstand a few type-I ELMs and/or disruptions via the vapor shielding effect. Accordingly, sets of Si-W test buttons were fabricated and exposed in the DIII-D lower divertor. We found that when the Si-W buttons were exposed to a few DIII-D vertical displacement event disruptions, tungsten-silicide was formed which melts at 1414°C. This clearly indicates that the Si-W combination cannot be used as a transient tolerance surface material, since the W surface can be damaged. Even when Si is used as a wall conditioning material the Si-W surface temperature should be operated at much lower than 1400°C.

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1. INTRODUCTON

C, Be, W and Mo are commonly used surface materials in operating tokamak experiments. For the ITER design, the guidance is to apply a Be armor onto the plasma facing chamber surface and W or the combination of C and W are to be used at the divertor [1]. For long burn DT fuel testing devices and DEMO, when the selection of chamber wall material is considered, the additional requirements of steady-state operation and tolerance to radiation damage from neutrons and charged particles will have to be taken into account. A Be armor will not be suitable due to radiation damage (dimensional instability, gas production and excessive increase of T inventory) [2,3]. Similarly, carbon tiles will not be suitable for the divertor surface due to high physical and chemical sputtering rates, radiation damage (dimensional instability and reduction of thermal conductivity) of the material and the potential for large retention of tritium [3]. The commonly accepted material for DEMO application is tungsten. Unfortunately, W could also suffer significant radiation damage from helium ion implantation, which could cause the formation of tungsten "fuzz" at the divertor surface [4–7] and surface morphology changes with the formation of blisters at the chamber wall [4]. Both the tungsten "fuzz" and the tungsten blisters could result in contamination of the plasma core.

For the development of advanced solid surface materials, it is difficult to foresee any low activation metallic alloy that can outperform W-alloy. However, for DEMO, in addition to potential surface damage from helium ions, W or any metallic surface is sure to melt to some extent under the thermal dump of transient events such as high power edge localized modes (ELMs) or from a disruption [8]. Therefore, in order to develop an acceptable robust plasma facing material (PFM), an innovative approach for maintaining an adequate amount of low-Z material for vaporization to handle a limited number of transient events was proposed [9]. When a sufficiently large surface area is filled with Si in the W surface, there is a possibility that this design would allow for the possibility of protecting the W-substrate from the thermal dump of high power ELMs or disruptions via the vapor shielding effect [10].

2. VAPOR SHIELDING EFFECT

The vapor shielding effect to protect the W substrate has been modeled using the HEIGTS [11] comprehensive simulation package. The modeling results show that for an ITER-like disruption on a boron/tungsten surface, the thermal energy will be absorbed by vaporizing B and most of the energy would be radiated away from the bulk material. The preliminary analysis showed that a thin layer of B will quickly evaporate and form a shielding layer to protect the W underneath. Similar results were projected for Si. This was credible since the melting point for B, Si and W are 2027°C, 1414°C and 3380°C, and corresponding boiling points are 3802°C, 2480°C and 5727°C, respectively. Based on the large difference of these temperatures, we projected that the infiltrated B or Si would be vaporized before significant damage to the W-surface would occur. From the energy balance between deposited energy, B vaporization and subsequent radiation, the estimated B layer removed per disruption, would be about <10 μm thick. Therefore, a net B thickness of 1 mm could take a few disruptions without excessive damage to the W-surface. Similar results were projected for Si but would have to be demonstrated by modeling. Si could be even more effective in protecting W due to its radiation properties compared to those of B. We have been attempting to demonstrate this disruption tolerant characteristic of Si in DIII-D.

3. DEVELOPMENT HISTORY

We initiated the project of the low-Z material loading on a W surface in 2007. In 2008 we acquired from Ultramet, the 1 in. diameter W-mesh disc shown in Fig. 1(a). When we tried to melt B at around 2000°C into the W-mesh disc, the sample was cracked and completely destroyed as shown in Fig. 1(b). In 2009, in order to get controlled porosity and pure W material samples, we switched to the use of an inch size W-disc as shown in Fig. 1(c). With the trial disc sample, we exposed the sample in DIII-D during vessel boronization, and we confirmed that the typical B-coating on the W substrate at the lower divertor was about 0.75 μm thick. The B-coated sample is shown in Fig. 1(d). During the same period, in order to avoid the possible necessity of isotopic de-tailoring of the neutron absorbing ^{10}B in a D-T device, we switched to the lower melting point Si as the low-Z material. We again ran into difficulties when we tried to melt Si into the holes of the W-disc; the disc was again destroyed by breaking into pieces. We suspected at that time that this failure was due to the mishap in the control of the oven temperature during the melting process of Si at 1414°C. In 2010, we continued the effort with the use of smaller 6 mm diameter buttons with indentations as shown in Fig. 1(e). We tried to fill the W-indentations physically at controlled temperature; the empty and filled buttons are shown in Fig. 2(a,b). The buttons were covered with relatively loose Si powder. We then exposed the filled buttons to four plasma discharges and one thermal dump at the divertor by using the DiMES system in DIII-D [9]. No thermal deposition had landed directy on the DiMES sample. Nothing much had happened to the buttons except that the loose Si on top of the buttons was removed as shown in Fig. 2(c,d). At the same time, the small amount of Si was eroded and distributed around the DIII-D vessel, but it had not caused any noticeable change to the plasma performance. In 2011, we fabricated W-buttons with both indentations and with the slots as shown in Fig. 1(e) and collaborated with Ultramet to fill the indentations and slotted spaces with Si via chemical vapor deposition (CVD). It should be noted that during the first round of W-button fabrication, the furnace temperature overshot during the CVD silicon process. The buttons were again completely destroyed by breaking into pieces as shown in Fig. 1(f–h). The upper temperature during the mishap is not known since the thermocouple also failed, but the temperature was at least ~1400°C for a few minutes. We then continued to prepare additional sample buttons using better temperature control. To assure the attachment of the Si onto the W-surface, the buttons were also first coated with AlN in order to reduce the impact of mismatch in the coefficient of thermal expansion between Si and W. We then exposed the DiMES module with the seven material buttons (five W buttons with indentations and slots, three of which filled with Si, one flat W button and one graphite button, as shown in Fig. 3(a) to six vertical displacement event (VDE) discharges.

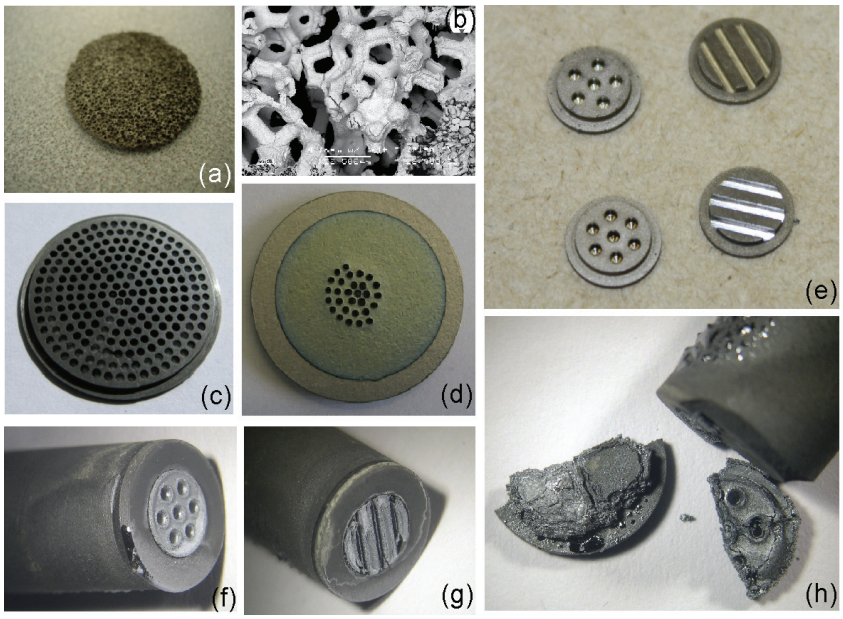

Fig. 1. Different W samples and buttons used in the study. (a) 1-in. diam. W mesh, (b) damaged W mesh, (c) 1-in. diam. W disc, (d) B coating on W, (e) 6 mm buttons with indentations and slots, (f) W indentation button Si-filled fixture, (g) W slots button Si filled fixture, (h) destroyed Si filled W button.

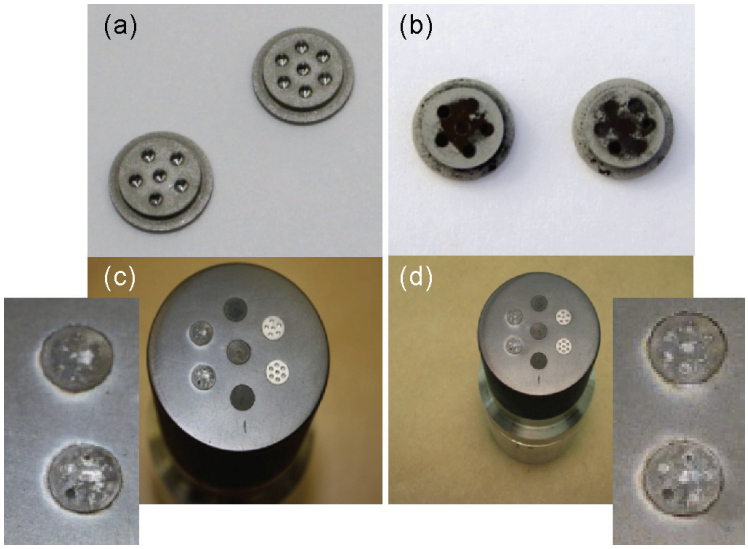

Fig. 2. Si-filled buttons were exposed to plasma discharges at the divertor. (a) W buttons with 1 mm indentations, (b) Si filled W-buttons, (c) sample exposed to four lower single null (LSN) discharges (shots 142641–142644), (d) sample exposed to one additional disruption (shot 142706).

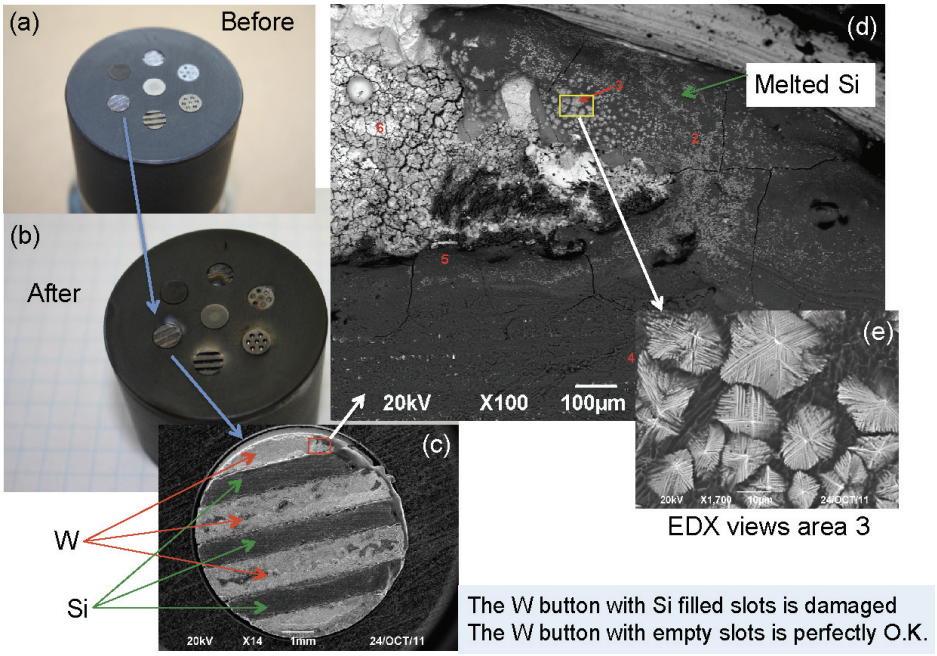

Fig. 3. Six VDE exposures indicating formation of Si-W eutectic. (a) DiMES module before exposure, (b) DiMES module with after exposure, (c) Si-filled W-slot button after exposure, (d) higher resolution of melted Si area, and (e) crystalline structure of W-Si.

4. VDE EXPOSURE IN DIII-D

The disruption group at GA was able to study VDE disruptions by turning off the disruption control feedback and giving the plasma a slight downward kick with shaping coils. We were able to repeat plasma shots and with repeatable control for the study of disruption mitigation [12]. VDEs are believed to be able to simulate near worst-case-scenarios for disruption heat loads. It will be most suitable to study the disruption heat loads striking the inner wall and divertor shelf, where the DiMES surface is located. Before the initiation of the disruption, the plasma was operating at a plasma current of ~1.3 MA. Six VDEs with initial energy (magnetic + thermal) ~2 MJ and peak deposited heat fluxes between 30 and 45 MW/m^2 were dumped onto the outboard divertor in the time frame of 5 to 25 ms. The locations of the landed plasma was modeled by JFIT [13] and the heat flux to the lower divertor was estimated from changes in IR camera brightness. The peak heat flux to the lower divertor shelf, where DiMES located, was also measured by Langmuir probes.

5. RESULTS

The DiMES module with Si-filled W-buttons is shown in Fig. 3. The module was exposed successfully to six well-controlled VDE exposures. Optical and SEM images of the DiMES module and buttons before (3a) and after (3b) the exposure are shown in Fig. 3. The most informative detail is shown at the right top corner of the Si-filled slotted button in Fig. 3(c). We can see the once melted Si at the edge of the button shown in Fig. 3(d). Upon closer examination, we can see the crystalline structure from the EDX area 3 view on top of the solidified but once melted Si as shown in the Fig. 3(e) on the right. When compared to the composition of materials at different locations of the melted region as shown with EDX analysis Table 1, one can identify the material composition of area 3, which has a composition of 49.31 wt% of Si, 41.11 wt% of W and 9.57% of C. For our sample, the C is from the graphite sample and background impurities in DIII-D. When compared to the Si-W phase diagram [14], the composition is very close to the Si-W mixture of 45.7 wt% of W, which melts at 1850°C. This composition of Si and W is a strong indication that the indicated location had gone up to the temperature of ≥1850°C [14]. With this identification, the explanation for the previous difficulties during the loading of B or Si onto W became clear. The samples were destroyed due to the formation of respective B-W and Si-W low melting point compounds at local temperatures. For B-W, different low melting point eutectic composition can begin to form at >1970°C, and for Si-W eutectic it can be formed at >1414°C, and the kinetics of such formation is very fast.

TABLE 1
EDX Analysis Showing Material Composition at Different Locations of the Si-W Button

Spectrum	C	N	O	Al	Si	W	Total
DiMES area 1	14.24				86.35	0.0	100
DiMES area 2	21.45			0.38	69.56	8.61	100
DiMES area 3	9.57				49.31	41.11	100
DiMES area 4	32.31		13.59	0.58	53.52		100
DiMES area 5	27.10		3.01	1.99	68.00	0.0	100
DiMES area 6	20.57	7.98	19.77	4.99	7.05	39.63	100
DiMES area 7	33.97		7.75			58.28	100
DiMES area 8	46.21		5.43		12.05	36.31	100
Max.	46.21	7.98	19.77	4.99	86.35	58.28	
Min.	9.57	7.98	3.01	0.38	7.05	0.0	

All results in wt%.

6. CONCLUSIONS

PFM is a critical element of the high performance DT tokamak reactor design. Presently, solid W is the preferred PFM due to its low physical sputtering, high thermal performance at elevated temperatures, and high neutron fluence tolerant properties. Unfortunately, it will melt under type-I ELMs and disruption events. A potential remedy is the use of low-Z material in combination with W. With the use of a low-Z sacrificial material, like Si deposited on the W-surface, it could protect the W-substrate to withstand a few type-I ELMs and/or disruptions without serious damage to the W-surface via the vapor shielding effect. Accordingly, sets of Si-W test buttons were fabricated and exposed in the DIII-D lower divertor with the goal of demonstrating their possibility of transient tolerance under disruption. During different fabrication processes with the implantation of Si onto W, we found that when the sample temperature was to be around 1400°C, the sample was destroyed and broken into pieces. Furthermore, our results in exposing the Si-W buttons to six VDEs in DIII-D showed that part of the W surface was damaged. Upon examination with SEM and EDX, tungsten-silicide crystalline structure was found with a composition of 49.31 wt% of Si and 41.11 wt% of W, with a melting point of ~1850°C, which was most likely formed during the transient event of a few ms. This clearly indicates that the Si-W combination cannot be used as a transient tolerance surface material, since the W surface can be damaged at temperature of >>1400°C with the formation of Si-W eutectic and the kinetics of reaction is quite fast during the event of a disruption or type-I ELMs. This result also implies that if a transient tolerant surface design cannot be found, and to avoid metallic surface melting, the requirement on the avoidance of high thermal dump transient events like type-I ELMs and disruption for a tokamak will become much more stringent. Furthermore, this result also indicates that even when Si or B were to be used as the wall conditioning material for a W-surface to mitigate the transport of W to the plasma zone, corresponding operating temperature should not go over 1410°–100° = 1310°C and 1970°–100°C = 1870°C, respectively, in order to avoid the formation of low melting point eutectics.

REFERENCES

[1] G. Federici, *et al.,* J. Nucl. Mater. **313–316**, 11 (2003).
[2] D. S. Gelles, *et al.,* J. Nucl. Mater. **212–215**, 29 (1994).
[3] H. Bolt, *et al.,* J. Nucl. Mater. **307–311**, 43 (2002).
[4] D. Nishijima, *et al.,* J. Nucl. Mater. **329**, 1029 (2004).
[5] R. F. Radel, *et al.,* J. Nucl. Mater. **367–370**, 434 (2007).
[6] N. Yoshida, *et al.,* J. Nucl. Mater. **337–339**, 946 (2005).
[7] M. Baldwin, *et al.,* Nucl. Fusion **48**, 1 (2008).
[8] L. Linke, *et al.,* J. Nucl. Mater. **283–287**, 1152 (2000).
[9] C. P. C. Wong, J. Nucl. Mater. **390–391**, 1026 (2009).
[10] V. Safronov, *et al.,* J. Nucl. Mater. **290–293**, 1052 (2001).
[11] A. Hassanein, Fusion Eng. and Design **60**, 527 (2002).
[12] E. M Hollmann, *et al.,* Nucl. Fusion **48**, 115007 (2008).
[13] D. A. Humphreys and A. G. Kellman, Phys. Plasmas **6**, 2742 (1999).
[14] "Binary Alloy Phase Diagrams," Vol. 3, 2nd edition, edited by Thaddeus B. Massalski, ASM International, 1990.

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