

# A Combined PLC and CPU Approach to Multiprocessor Control\*

J.J. Harris, J.D. Broesch, R.M. Coon  
General Atomics  
P.O. Box 85608, San Diego, California 92186-9784

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## ABSTRACT

A sophisticated multiprocessor control system has been developed for use in the E-Power Supply System Integrated Control (EPSSIC) on the DIII-D tokamak. EPSSIC provides control and interlocks for the ohmic heating coil power supply and its associated systems. Of particular interest is the architecture of this system: both a Programmable Logic Controller (PLC) and a Central Processor Unit (CPU) have been combined on a standard VME bus. The PLC and CPU input and output signals are routed through signal conditioning modules, which provide the necessary voltage and ground isolation. Additionally these modules adapt the signal levels to that of the VME I/O boards. One set of I/O signals is shared between the two processors. The resulting multiprocessor system provides a number of advantages: redundant operation for mission critical situations, flexible communications using conventional TCP/IP protocols, the simplicity of ladder logic programming for the majority of the control code, and an easily maintained and expandable non-proprietary system.

## INTRODUCTION

EPSSIC controls the performance of the ohmic heating coil power supply (E-Supply) and the sequencing of the high current switches associated with that power supply on the DIII-D tokamak. The E-Supply itself includes a main control cabinet which manages the parallel operation of the four identical local modules containing interlock and regulation circuitry. The main control cabinet of the E-Supply accepts remote signals from EPSSIC and CAMAC systems to turn on and invert the power supply twice during one plasma discharge.

The EPSSIC control system had been in operation since the late 1970's and consisted of analog and digital circuitry designed in house. The relay ladder logic and analog input based approach was used for shot sequencing, interlocks, mode, and high current switch control. EPSSIC accepts a number of signals from other systems that are an integral part of the E-Supply interlock and control scheme.

While the former EPSSIC system had been reliable for many years, we found not only had we reached the end of the useful life of the components; the increased cost of maintenance did not warrant the continuation of merely repairing the system. Some of the system components were obsolete. Due to the location of the equipment, remote monitoring and diagnostics were impossible without suspending tokamak operations.

Additionally, changes, improvements or upgrades were nearly impossible to perform, especially during the brief maintenance periods. This inflexibility, the need to improve diagnostics, and obtain better control led to the decision to redesign EPSSIC. A combined PLC and CPU based system seemed to be the best fit with the anticipated improvements in the DIII-D control system.

## UPGRADE STRATEGY

There were a number of objectives in designing the new EPSSIC system. The first objective was to implement the functionality of the original EPSSIC with a platform that had a low maintenance cost. Second, additional functionality should be incorporated, and the upgraded configuration should have improved reliability and flexibility. Additionally, the system should be designed so future expansions could easily be accommodated. The EPSSIC system is located in the E-Supply building which has controlled access and is off limits to personnel during plasma operations. Therefore, diagnosing system problems with the former EPSSIC meant temporarily ceasing operations and sending personnel out to the site. The final design requirement was to improve communication between EPSSIC and the main DIII-D control room and computers. Further, we also needed to assure the continuance of protection of personnel, the DIII-D tokamak and coils, and the associated high current (170 kA) switches and power supplies.

The approach should be based on standard factory automation principles which includes fail safe equipment and redundant features. Additional protection and redundancy should be implemented with PLDs (Programmable Logic Devices), providing us with the necessary execution speed and flexibility for future development. A platform was needed that was easily maintained, modular and expandable, requiring an open bus architecture. Multibus, STD, VME and VXI were all considered. However, the VME system was chosen for its high performance and reliability, relatively low cost, and the availability of a wide variety of modules. High speed, optically isolated communications were a requirement. High mean time between failure and long hardware life cycles were also important. The final design would make extensive use of off-the-shelf hardware and software for both ease of implementation and maintenance.

A combination of VME PLC and VME CPU technology was chosen as the heart of the system (Fig. 1). The PLC would easily replace the hardwired relay ladder logic used in the previous version of EPSSIC and provide a simple and easy way to implement changes or upgrades. The CPU would give

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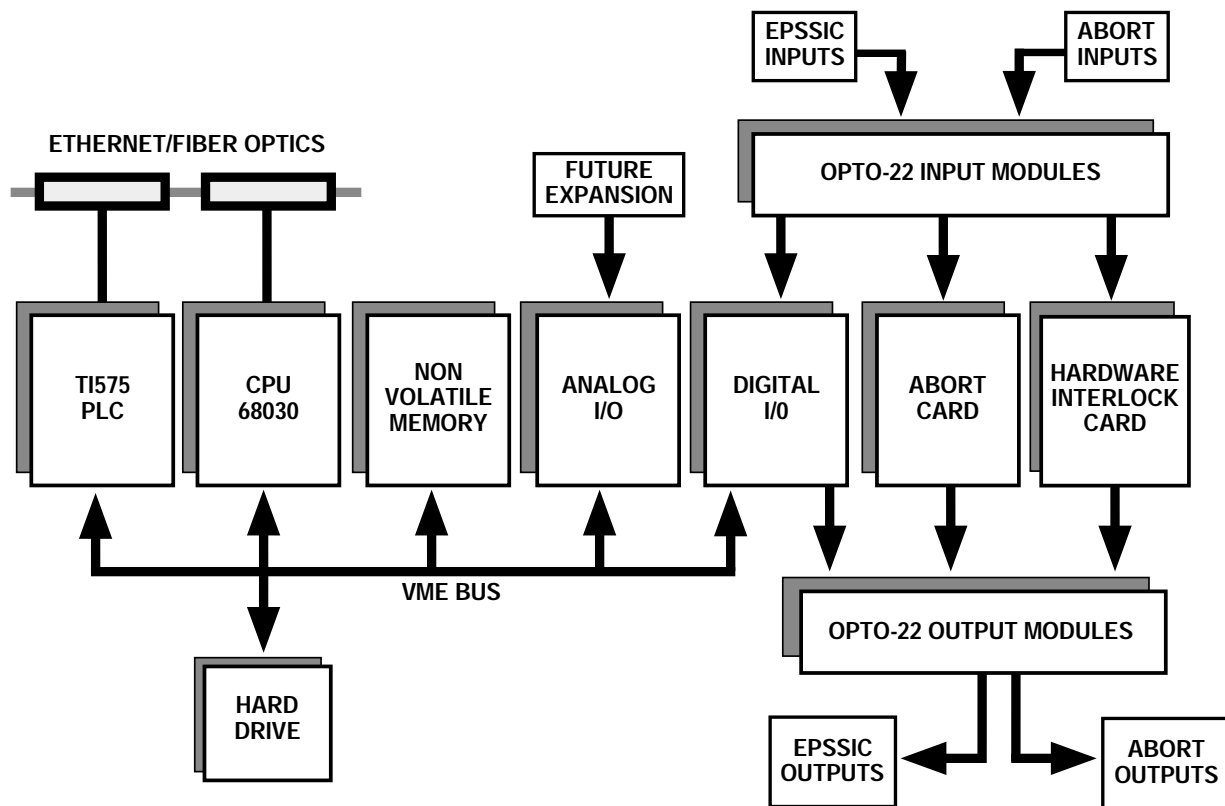


Fig. 1. EPSSIC VME system block diagram.

us the required execution speed and provide redundant operation for critical situations. Additionally it would provide a platform for the development of a real time control system and user friendly operator interface. Both would provide enhanced communication using TCP/IP and RS232 protocols over a fiber optic network. Because of the variety of different voltage levels on the incoming signals to EPSSIC, and the need for voltage and ground isolation, signal conditioning modules were specified and installed for direct interface to VME I/O modules.

#### HARDWARE UPGRADE CONFIGURATION AND DESCRIPTION

In the final design a Siemens 575 VME PLC was chosen as the main element for the EPSSIC system. It was the only PLC available at the time that would work with third party VME hardware. The 575 would replace the existing hardwired relay logic with a user written program that could easily be changed or modified. The 575, however, must reside in one specific location, thus making it the VMEbus master and arbiter. We were unable to find a PLC that would operate as a slave. A Matrix Corporation 68030 CPU was selected as the additional slave processor. The Matrix CPU was chosen because it had the capability of working in the multiprocessor environment and support was made available to us on the task of integrating the CPU, VME I/O modules, and software into a working system.

The 575 PLC addresses up to 8192 I/O points in a mix of analog and digital signal types. It can execute all of the standard PLC commands and perform PID loops. It was unique in its ability to connect to standard PLC and VME I/O hardware. The 575 can also address global memory over the VMEbus. Communication is made simple using RS232 protocols. Programming the ladder logic and VME data transfer routines is easily achieved using the Siemens TISOFT language. The scan and execution time is less than 5ms, but there are times when that is too slow for some critical control sequences. Therefore, in addition to adding a CPU, we designed a Hardware Interlock Card (HWI) to handle those situations in conjunction with the CPU. The HWI Card functions will be discussed later.

The CPU is a Motorola 68030 based processor conforming to the VMEbus standard. It is configured as a slave processor, however, direct communication with it is possible via an Ethernet connection. The CPU, chassis, modules and software were delivered as a turnkey system; meaning all of the integration, except for the PLC, was performed at the factory. The integration included memory mapping for the 4 Mb of battery backed RAM and disk drives, Ethernet connectivity, and I/O mapping. The CPU has interrupt handlers and a watchdog timer for error checking and reporting. Since the CPU would be used for control functions, health monitoring, and communications, a multi-tasking real time operating system was needed. OS9 was

chosen for the CPU operating system. It is a multitasking, UNIX-like, real time operating system. It supports Ethernet TCP/IP protocol and most application software written in C can be recompiled to run on OS9. This operating system can be run from the VME compatible, removable hard disk (which is used primarily for program and operator interface development) or EPROM. This feature is especially attractive to us because of the strong transient magnetic fields in the E-Supply building during tokamak operations.

The systems reporting to EPSSIC and the VME processor system have varying voltage levels. Because of this and the need for voltage and ground isolation between the different systems, we chose to use I/O signal conditioners on the front end. All incoming and outgoing signals were adapted to the 5 V levels used by the VME I/O modules by using the Generation 4 OPTO-22 system. Twenty-four channel I/O mounting racks were installed to accept a variety of input and output modules. These mounting racks interface easily and directly to the VME I/O modules via 50 pin ribbon connectors. All OPTO-22 modules have at least 4000 V optical isolation. They provide fast turn-on and turn-off capabilities with transient free switching.

### SYSTEM UPGRADE PROCEDURE

The task of changing over to the new system could only be accomplished during an extended shutdown period. It was desirable to restore the old EPSSIC system in a matter of

days at any point during the upgrade process. Therefore we chose to install an additional cabinet and wire all EPSSIC signals in parallel to the new system, maintaining the old wiring and functionality while installing and programming the new.

While EPSSIC provides shot sequencing, mode and switch controls and shot cycle inhibits; it is tied very closely to an abort system which will actually stop a shot in progress, command the high current switches to change modes and shut down the power supply (Fig. 2). ABORT protects all power supplies and coils because it is interlocked to overcurrent, coil cooling and coil stress systems. It also provides facility protection in the event of a fire alarm trip and personnel protection in case of a breach in access control. ABORT is tied to the EPSSIC baking mode, disabling all power supplies when vessel baking is selected. It was decided during the upgrade process to include the ABORT/EPSSIC interface because it was far easier to upgrade to the new platform, than to work around the old.

The Hardware Interlock Card was designed to complement the EPSSIC and ABORT systems and to provide command series redundancy during critical times during the shot sequence and especially to protect the high current switches (Fig. 3). The HWI Card must ensure a benign condition for the high current switches in the event of a fault or major component failure. The HWI Card can issue an ABORT or inhibit command independently of the PLC and CPU, especially if the HWI Card determines that either of these

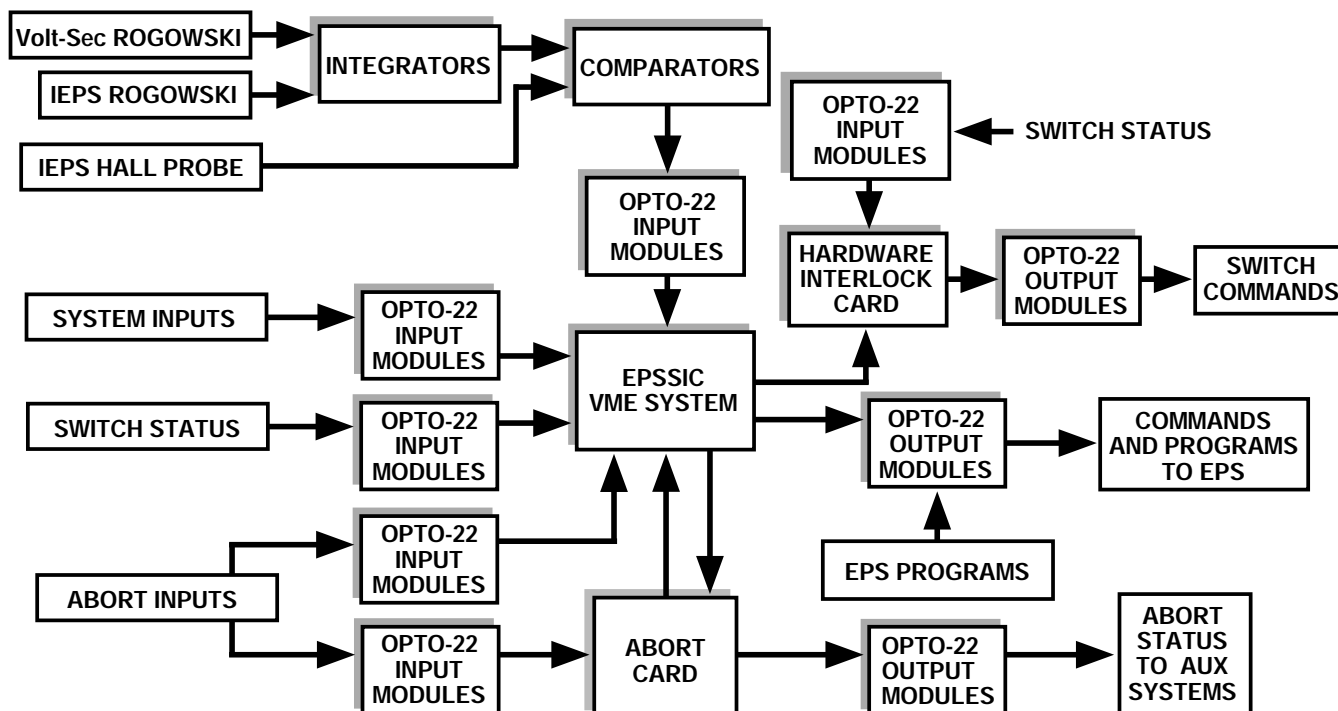


Fig. 2. EPSSIC functional block diagram.

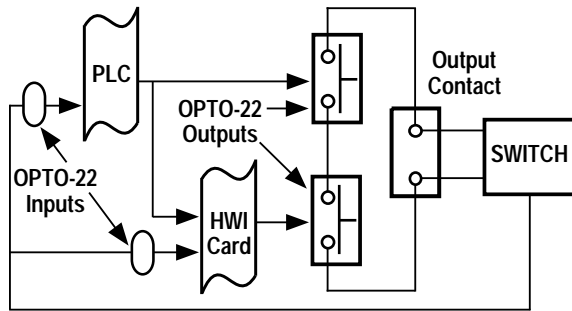


Fig. 3. Typical series redundant circuitry.

two components are generating spurious commands or if they have not periodically reset a watchdog timer that is resident on the HWI Card. The HWI Card monitors high current switch settings for legal and illegal conditions and will issue an ABORT in the event of hazardous switch positions in addition to preventing illegal switch setting combinations in the first place. It makes extensive use of PLDs to accomplish that goal. Finally the HWI Card proves to have a much faster response time (microseconds vs. milliseconds) during fault conditions than the PLC has.

The comprehensive and extensive design upgrade required a great deal of thought and planning. An extensive test plan was developed to cover every detail of the upgrade process up to and including using the system with the coils energized. The test plan included checkout of all the wiring, simulating inputs and outputs at the system level, and checks involving sequencing and timing. The latter was done of course with the PLC ladder logic program in place. Additionally source and destination checkout was performed on all systems interfacing to EPSSIC and ABORT. Finally, shot simulations were performed and eventual testing with the power supplies commenced before the final commissioning of the system.

#### OPERATING EXPERIENCE AND FUTURE PLANS

The EPSSIC system, in its upgraded configuration, was commissioned and on-line for the operating period following our extended shutdown. It has performed well and has given

us many new tools and diagnostic capabilities that we never had before. For example if a shot times out it is possible to view the PLC program and determine exactly where the shot was terminated and why. We are now able to view the I/O remotely and make program changes on line for special shot sequences. The system has proved to be reliable and minor upgrades have already been performed during our routine maintenance periods. The modularity of this system lent itself to this. Thus far there has been virtually no system maintenance needed.

There are a number of upgrades which can be done in the future. One includes analog signal conditioners for importing switch current and coil current signals into the EPSSIC VME system. This would allow us to gain more control and status monitoring of the system. Digital comparators will be installed allowing the PLC and CPU to monitor EPSSIC integrator and hall probe outputs, thus controlling switch firing sequences more closely.

#### CONCLUSION

The EPSSIC system in its upgraded configuration has proven to be an enhanced, reliable system for both operating the E-Supply and its associated hardware. The multi-processor approach has proven to be the best of both worlds because it gives us the ease and flexibility of programming and reliability. The PLC component made the transition from the old to new system straightforward and the CPU component gives us the redundancy and faster execution speed needed for critical sequencing situations. The I/O is shared between the processors and resides on the VMEbus with them. The HWI Card complements the EPSSIC and ABORT systems by providing series redundancy during critical sequences. All inputs are buffered for voltage and ground isolation for increased noise immunity and safety. Flexible TCP/IP and RS232 communication is now achieved to the remote site making diagnostics and status more readily available. The modularity of the system makes it easier to maintain, and upgrades can be performed with little or no down time. The operator interface is now much more user friendly and allows for 'one button' resets and sequencing. All hardware is off-the-shelf industry standard thus achieving our goal of a true non-proprietary system.