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14.45 High-speed data acquisition system based on FPGA for Tokamak

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The Experimental Advanced Superconducting Tokamak (EAST) device aims to achieve steady-state operation and long pulse discharge over 1000 seconds. The sampling rate of diagnosis systems usually ranges from 10 KSps to 10 MSps. With the requirement of some particular diagnosis, high-speed acquisition is needed. An embedded system based on FPGA with high-speed, long-time data acquisition is proposed in this paper. Cyclone FPGA EP4CGX30F484 is used as the master chip, and an ATMEL's ADC chip is used to complete analog-to-digital conversion. The acquisition system is made up of 4 pieces of ADCs. The clock signals in the system are generated by LMK61A2 clock module controlled by FPGA to realize 4 channels alternate samples of ADCs. The acquired data is written into the disk array through PCIE interface, and then uploaded to the data server. The system can process eight different signals synchronously. A number of such system units can be used to collect more channel signals. The experimental result shows that the system can reach 80 Msps and the sampling precision can reach 12-bit with the 1500s continuous sampling. The system integrates signal conditioning, data acquisition and data processing into the single board, and provide a high integration and portability level architecture.

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