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2.18 Real-Time Digital Phase Demodulator for the ITER Toroidal Interferometer and Polarimeter (TIP)

Monday, 16 April 2018 10:46 (120)

The ITER TIP system requires real time phase demodulation of several radio-frequency (RF) signals to provide accurate electron density measurements essential for plasma control. This is accomplished using a four-channel digital phase demodulator (DPD) constructed using a high-density Field Programmable Gate Array (FPGA) coupled to high-speed analog-to-digital converters (ADC). The DPD samples signals from four optical detectors each containing frequencies at 4, 40, and 44MHz. Digital signal processing (DSP) techniques are used to separate the three frequencies and measure their phase. Two versions of DPDs have been constructed and tested on the DIII-D TIP system. The first was fabricated using a Xilinx Kintex-7 FPGA development board, a high-speed ADC module from Analog Devices, and custom hardware from Palomar Scientific Instruments. The second was assembled using ITER-approved components from National Instruments. The FPGA implementation for both versions was designed using Matlab System Generator and the VHDL programming language. Both systems have been shown to provide phase measurements with better than 0.01° accuracy at 500kHz bandwidth. Work supported by U.S. DOE Contracts DE-AC-02-09CH11466 and DE-FC02-04ER54698.

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